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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/764,152 | 01/23/2004 | Dennis E. Dudeck | 2-5-33-6 | 8149 |

7590 08/12/2005

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| EXAMINER | |
|---|---|
| NGUYEN, TAN | |
| ART UNIT | PAPER NUMBER |
| 2827 | |

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/764,152 | DUDECK ET AL. |
| | Examiner | Art Unit |
| | Tan T. Nguyen | 2827 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The Information Disclosure Statement submitted by Applicant on January 23, 2004 has been received and fully considered.

2. The Formal Drawings submitted by Applicant on March 10, 2004 have been received.

3. Applicant is advised to provide the serial numbers of the copending applications cited in the present application.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Rogenmoser et al. (U.S. Patent No. 6,430,099).

Regarding claims 1 and 13, Rogenmoser et al. disclosed in Figure 1 a Read Only Memory (ROM) [10] comprises a ROM array [12], which includes a first partition [14A], a second partition [14B], a third partition [14C], the partitions are coupled to an address decoder [16], a bit line precharge circuit [20] and an output circuit [22]. The precharge circuit [20] is coupled to a partition selector circuit [18] (column 2, lines 58-63), wherein the partition selector circuit [18] is coupled to receive an attribute input [ATTR] (column 3, line 13-14). The partitions are each coupled to separate sets of bit line conductors, both the bit line precharge circuit [20] and the output circuit [22] are coupled to each of the bit line conductors from the partitions [14A-14C] (column 2, line 67 to column 3, line 6). Rogenmoser et al. disclosed generally, the bit line precharge circuit [20] is

configured to precharge one of the sets of the bit line conductors corresponding to one of the partitions of the ROM array [12] in response to that partition being selected for a read of ROM [10]. Furthermore, the bit line precharge circuit [20] is configured to not precharge other ones of the sets of bit line conductors corresponding to the remaining partition (column 3, lines 15-21). Rogenmoser et al. disclosed a read operation of the ROM [10] wherein prior to initiating the read from the partitions [14A-14C], the bit line precharge circuit [20] precharges the bit line conductors corresponding to the partition being read (column 4, lines 23-25). After the precharge, the precharge circuit [20] deactivates the precharge circuits therein and the partition being read may evaluate to determine the value output from the ROM [10] (column 4, lines 30-32).

Regarding claims 7, 13, 6, 12, 18 and 24, Rogenmoser et al. disclosed the partition selector circuit [18] provides the Pchg[2:0] input signals to the precharge circuit [20 to control which of the sets of bit line conductors are precharged and which are not (column 3, lines 39-41). The partition selector circuit [18] would be considered as the claimed decoder.

Regarding claims 2, 8, 14 and 20, the set of bit line conductors in each partition [14A-14C] would be considered as the claimed subset of columns.

Regarding claims 3, 9, 15 and 21, Rogenmoser et al. disclosed the partition selector circuit [18] may generate the Pchg[2:0] signals responsive to the ATTR input. The ATTR input may be additional address bit separate from the address provided to the address decoder [16] (column 4, lines 50-55).

Regarding claims 4-5, 10-11, 16-17 and 22-23, the sets of bit line conductors in the partitions [14A-14C] would be considered as the claimed sub-arrays, wherein only the set of bit line conductors of the selected partition are precharged, and the remaining partitions are not precharged (column 4, lines 23-27).

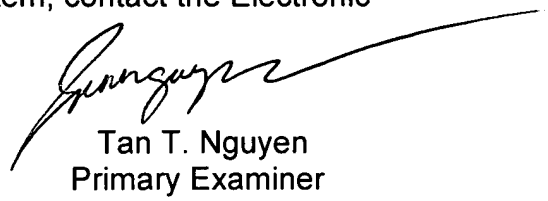
6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Komarek et al., Jung and Hidaka are cited to show memory device having sequential precharge. Cho and Sood are cited to show memory devices having plurality of sub-arrays and the sub-arrays are alternately precharged.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen
Primary Examiner
Art Unit 2827
August 11, 2005